Claim 20 is directed to a method for storing video data in a memory circuit that has a plurality of arrays. The method includes "segmenting a plurality of pixels representing one horizontal line of an image ... into a plurality of pixel groups" and "storing data representing each of said plurality of pixel groups, respectively, in a row of a plurality of non-adjoining arrays in the memory circuit." For instance, in the example shown in Fig. 4, where adjacent arrays have consecutive numbers, data for the first 32 pixels in scan line 0 can be stored in row 0 of array 0, the next 32 pixels in row 0 of array 2, and so on. As described in the specification, in instances where pairs of adjacent arrays in the memory circuit share sense amplifiers, storing data for adjacent groups of pixels in non-adjacent arrays improves memory access time by allowing memory cells for adjacent pixel groups to be active at the same time.

May is directed to storing pixel data in memory in a tile format, where the tile shape (height and width) may be dynamically altered depending on the nature of the data. A circuit is provided to convert a pixel location to a memory address (May, Abstract). Pixels within a tile are stored at contiguous addresses, thereby reducing the number of row accesses required (Figs. 3A-B; col. 3, lines 7-30).

May does not disclose storing the data in non-adjoining arrays, as recited in claim 20. The rejection, while acknowledging that May does not disclose this feature, asserts that it would be an obvious modification. To establish obviousness, the rejection relies on disclosure in May to the effect that accesses to data in different columns of the same row are faster than accesses to data in different rows (col. 1, lines 47-50).

Applicant respectfully submits that motivation to modify May to use non-adjoining arrays has not been established. While it is generally true, as May discloses, that column access is faster than row access within an array, this suggests only that the total number of row accesses for each tile should be minimized. In a case where a tile (or any other group of pixels) requires more than one row of memory, May provides little disclosure regarding which rows to use. The only embodiments disclosed compute contiguous memory addresses for pixels within a tile, so that data for adjacent pixels is stored in adjacent rows within the same array. As best understood, May does not disclose

or even suggest that switching from a row of a first array to a row of a second array has any advantage over switching to a new row in the same array, let alone that switching between *non-adjoining* first and second arrays, as recited in claim 20, has an advantage.

One of ordinary skill in the art would recognize that modifying the address-computation circuitry of May so that data for adjacent pixel groups was stored in non-adjoining arrays would increase the complexity of the circuitry. Nothing in May suggests that there is any advantage to be gained by such a modification; thus, one of ordinary skill in the art would not be motivated to modify the circuitry to use non-adjoining arrays. The existence of an advantage is apparent only in view of teachings of the present application regarding memory access to non-adjoining arrays, i.e., in hindsight. Use of hindsight to establish obviousness is inappropriate.

For at least these reasons, claim 20 is patentable over May. Further, claims 21-24, which depend from claim 20, are also patentable over May for at least these reasons.

Independent claim 25 recites a method for storing video data in a memory circuit. The method includes "dividing the display panel into a first half and a second half," "storing pixel data from the first half in odd numbered arrays ...," and "storing pixel data from the second half in even numbered arrays ...." In this method, data for adjacent pixels is stored in non-adjoining arrays, given that arrays are numbered consecutively. The rejection asserts that, since May discloses that tile size is a selectable parameter, it would be obvious to select half the display panel as a first tile and the other half as a second tile.

Even assuming arguendo that such a tiling would be obvious, claim 25 is nevertheless patentable. As explained above, May fails to disclose or suggest using non-adjoining arrays, let alone using odd numbered arrays for a first half of the pixels and even numbered arrays for a second half of the pixels. Therefore, claim 25 is also patentable over May.

Withdrawal of the rejection of claims 20-25 under 35 U.S.C. §103(a) is respectfully requested.

Submission of Appendix A

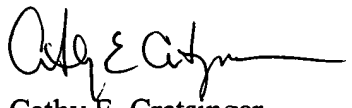
The Office Action stated that the article referred to as Appendix A was not received by the Examiner and requested that a copy be provided or that the reference be deleted. Filed herewith is a copy of the article referred to in the specification of the present application as Appendix A. As stated in the specification, this article describes "[a] specific video memory circuit which incorporates an exemplary embodiment of the present invention as well as other related circuit techniques."

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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